

## FEATURES

- 30MHz to 90MHz Tunability
- 240 Frequency Steps
- Constant Q, Two-pole Butterworth Bandpass
- 1W Power Handling
- 30µs Tuning Speed
- Serial/Parallel Modes
- -40C to +85C



## DESCRIPTION

The TS5010 series of TeraTune™ digitally programmable bandpass filters are available in various frequency ranges and bandwidths to help solve your CoSite receiver problems. They feature 1W power handling, low insertion loss, and frequency agility. The TS5010 is offered in both board-mounted and standalone SMA connectorized versions for ease of installation.

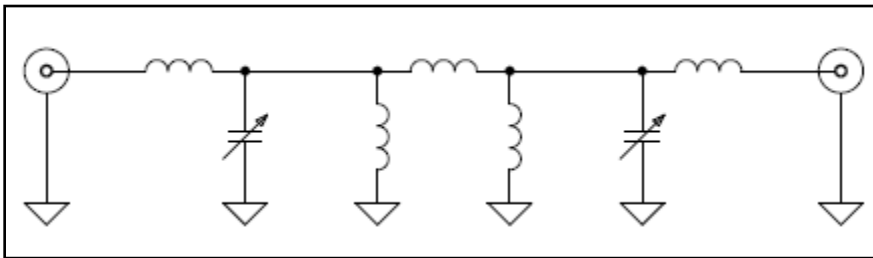


Figure 1: Equivalent Circuit

The TS5010 offers performance upgrades in an industry standard footprint. Designed from the ground up, these filters present a cost-effective alternative with enhanced features.

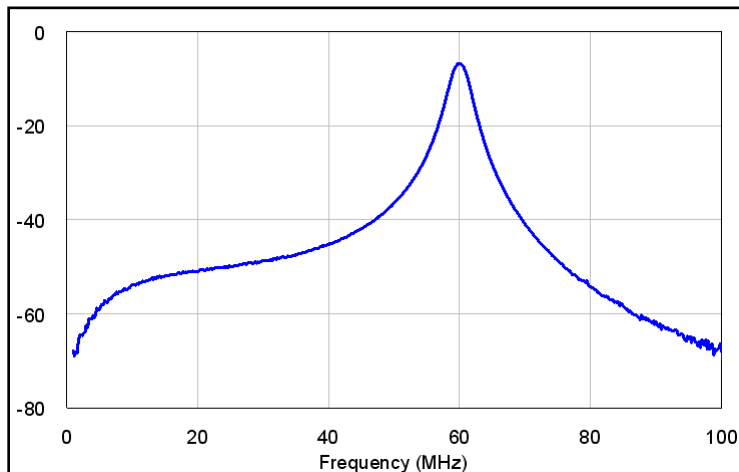


Figure 2: Typical Frequency Response

## PART NUMBERING

TS	-	Series	-	Range	-	Steps	-	BW	-	Control	-	Options
TS	-	5010	-	30-90	-	240 250	-	5 4 3	-	P S R	-	C

P = Parallel

S = SPI

R = Asynchronous Serial (RS-232)

C = Connectorized Package (SMA)

## RF PERFORMANCE

Parameter	BW	Symbol	Min	Typ	Max	Units
Input Impedance		Z <sub>O</sub>		50		Ω
In-Band 3 <sup>rd</sup> Order Intercept		IP3	40			dBm
In-Band Power	5.0 4.0 3.3	P <sub>IB</sub>		32 31 30		dBm
Out-of-Band Power		P <sub>OB</sub>	36			dBm
Insertion Loss	5.0 4.0 3.3	S21		5.0 6.0 8.0	6.5 7.5 9.5	dB
Shape Factor (30dB/3dB)		SF		6	7	
High Frequency Loss (2 x f <sub>0</sub> )	5.0 4.0 3.3	HFL	60 65 70			dB
Bandwidth Variation		BWV	-1	0	+1	%
Center Frequency Drift		F <sub>D</sub>			100	ppm/C

## POWER SUPPLY

Parameter	Symbol	Min	Typ	Max	Units
Power Supply Voltage	V <sub>CC</sub>	4.5	5.0	5.5	V
Power Supply Current	I <sub>CC</sub>	10		400	mA
Bias Supply Voltage	V <sub>BB</sub>	10		100	V
Bias Supply Current (quiescent)	I <sub>BB</sub>		4	5	mA

## ENVIRONMENTAL

Parameter	Symbol	Min	Typ	Max	Units
Operating Temperature	T <sub>O</sub>	-40	25	85	C
Storage Temperature	T <sub>S</sub>	-55		100	C
Relative Humidity	RH	0		95	%

## CONTROL INPUTS

Parameter	Symbol	Min	Typ	Max	Units
Input Low Voltage	V <sub>IL</sub>	-0.3	0	0.3V <sub>CC</sub>	V
Input High Voltage	V <sub>IH</sub>	0.7V <sub>CC</sub>	V <sub>CC</sub>	V <sub>CC</sub> + 0.3	V
Output Low Voltage (I = 10mA)	V <sub>OL</sub>	0		0.3V <sub>CC</sub>	V
Output High Voltage (I = -10mA)	V <sub>OH</sub>	0.7V <sub>CC</sub>		V <sub>CC</sub>	V

### TUNECODE

The frequency band is divided into equal steps with the TuneCode defined by the following formula. TuneCodes above 250 are reserved for special operations. Power save mode shuts off all PIN diodes for lowest power consumption.

$$TuneCode = Steps \cdot \left( \frac{f_{desired} - f_{min}}{f_{max} - f_{min}} \right)$$

Code	Operation
0 - 250	TuneCode
251	<reserved>
252	<reserved>
253	<reserved>
254	<reserved>
255	Power Save Mode

### PARALLEL MODE

In parallel mode, the TuneCode is specified per the input pins when the /STB line goes low. Once strobed, an internal processor looks up the required PIN diode control words and sets them accordingly. The PIN diode switch drivers take another ten microseconds to slew on or off, and the resulting bandpass is indeterminate during this time.

Parameter	Symbol	Min	Typ	Max	Units
Setup Time	t <sub>S</sub>	0			ns
Hold Time	t <sub>H</sub>	100			ns
Strobe Pulse Width	t <sub>W</sub>	25			ns
Access time from Strobe to +10dBm	t <sub>ACC</sub>			30	μs
Dwell Time	t <sub>DW</sub>	250			μs

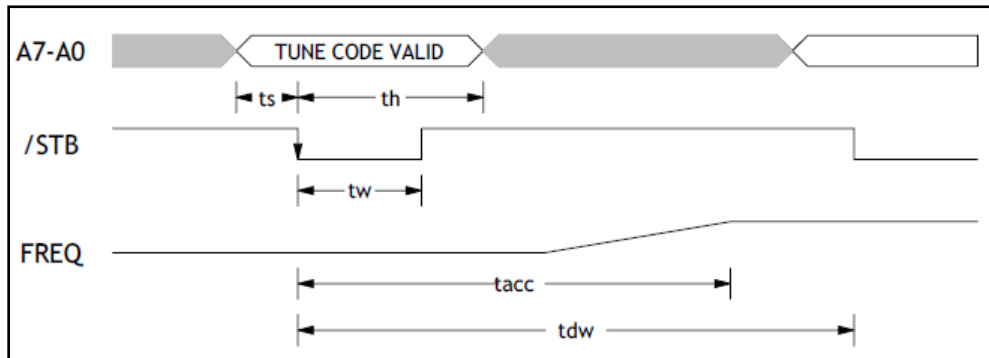


Figure 3: Parallel Mode Timing

### SERIAL (SPI) MODE

The TuneCode is clocked in serially one bit at a time, MSB first. Timing is synchronous and can be at any rate under the maximum clock rate of 5MHz. To start a sequence, the chip select line (/SS) is pulled low. Once /SS goes high, the internal processor begins the decoding process and sets the new frequency.

Parameter	Symbol	Min	Typ	Max	Units
Select Setup Time	$t_{CS}$	100			ns
Data Setup Time	$t_{DS}$	50			ns
Data Hold Time	$t_{DH}$	50			ns
Clock High Time	$t_{CH}$	100			ns
Clock Low Time	$t_{CL}$	100			ns
Access Time from Select to +10dBm	$t_{ACC}$			30	$\mu s$
Dwell Time	$t_{DW}$	250			$\mu s$

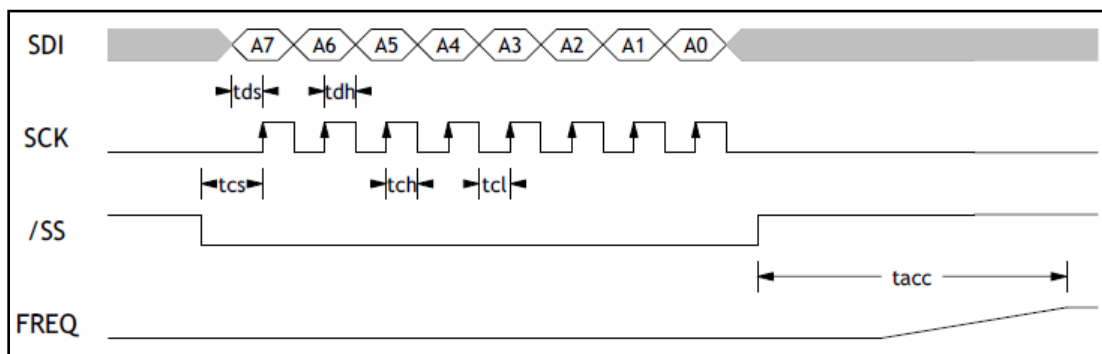


Figure 4: Serial Mode Timing

### RS-232 (ASYNC) MODE

The baud rate is fixed at 9600, 8N1. Voltage levels are TTL, with mark high, space low. Be careful not to use TuneCodes 253 and 254 as they are reserved for manufacturing and calibration purposes. Use of these codes may cause indeterminate results.

## PINOUTS

Pin	Name	Type	Description	Pin*
1	RF_IN	I/O	RF Input and Output	
2	GND		Ground	
3	GND		Ground	
4	VCC	I	+5V Supply	1
5	GND		Ground	2
6	A7	I	Tune Bit 7 (MSB)	3
7	A6	I	Tune Bit 6	4
8	A5	I	Tune Bit 5	5
9	A4	I	Tune Bit 4	6
10	RX		Receive RS-232 (Logic Levels)	
	A3	I/O	Tune Bit 3	7
	TX		Transmit RS-232 (Logic Levels)	
11	A2	I/O	Tune Bit 2	8
	SDO		Synchronous Data Out (SPI)	
12	A1	I	Tune Bit 1	9
	SDI		Synchronous Data In (SPI)	
13	A0	I	Tune Bit 0 (LSB)	10
	SCK		Synchronous Clock (SPI)	
14	/STB	I	Strobe (Parallel Load)	11
	/SS		Synchronous Select (SPI)	
15	GND		Ground	12
16	GND		Ground	13
17	VBB	I	+100V Bias Supply	14
18	GND		Ground	15
19	GND		Ground	
20	GND		Ground	
21	RF_OUT	I/O	RF Input and Output	
22	GND		Ground	
23	NC		No Connect	
-				
41				
42	GND		Ground	

\* SMA version

## MECHANICAL

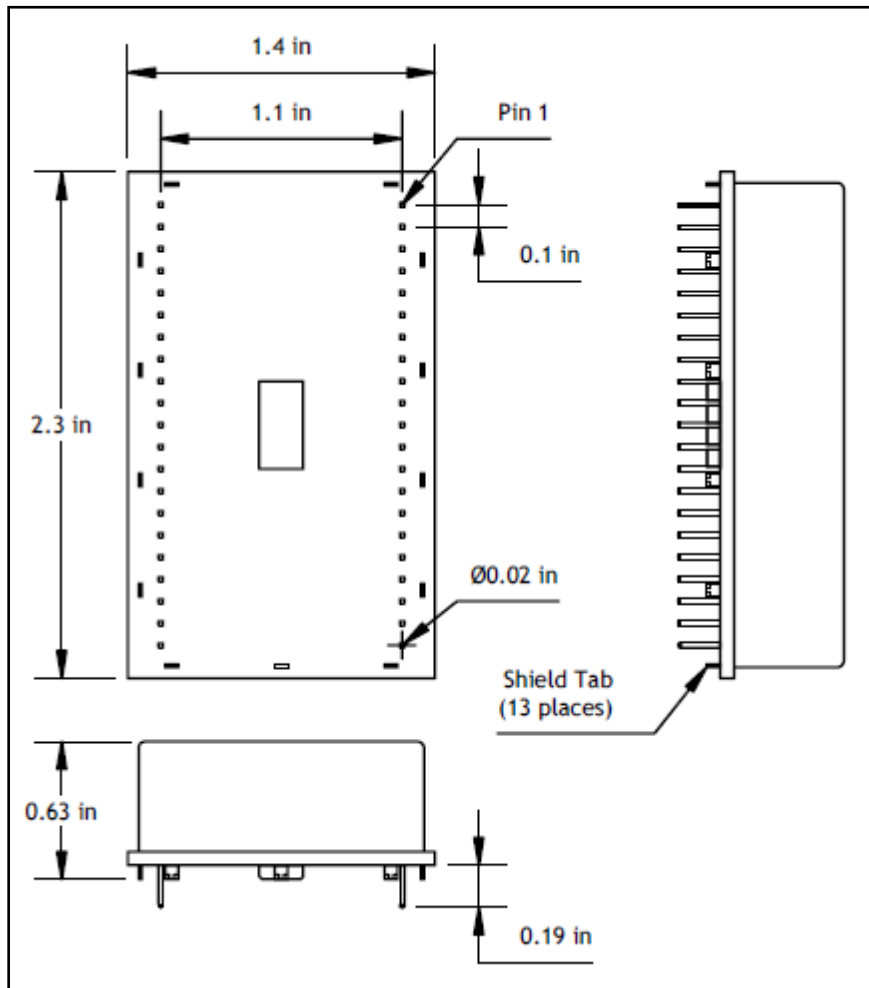


Figure 5: Package Dimensions, Bottom and Side Views

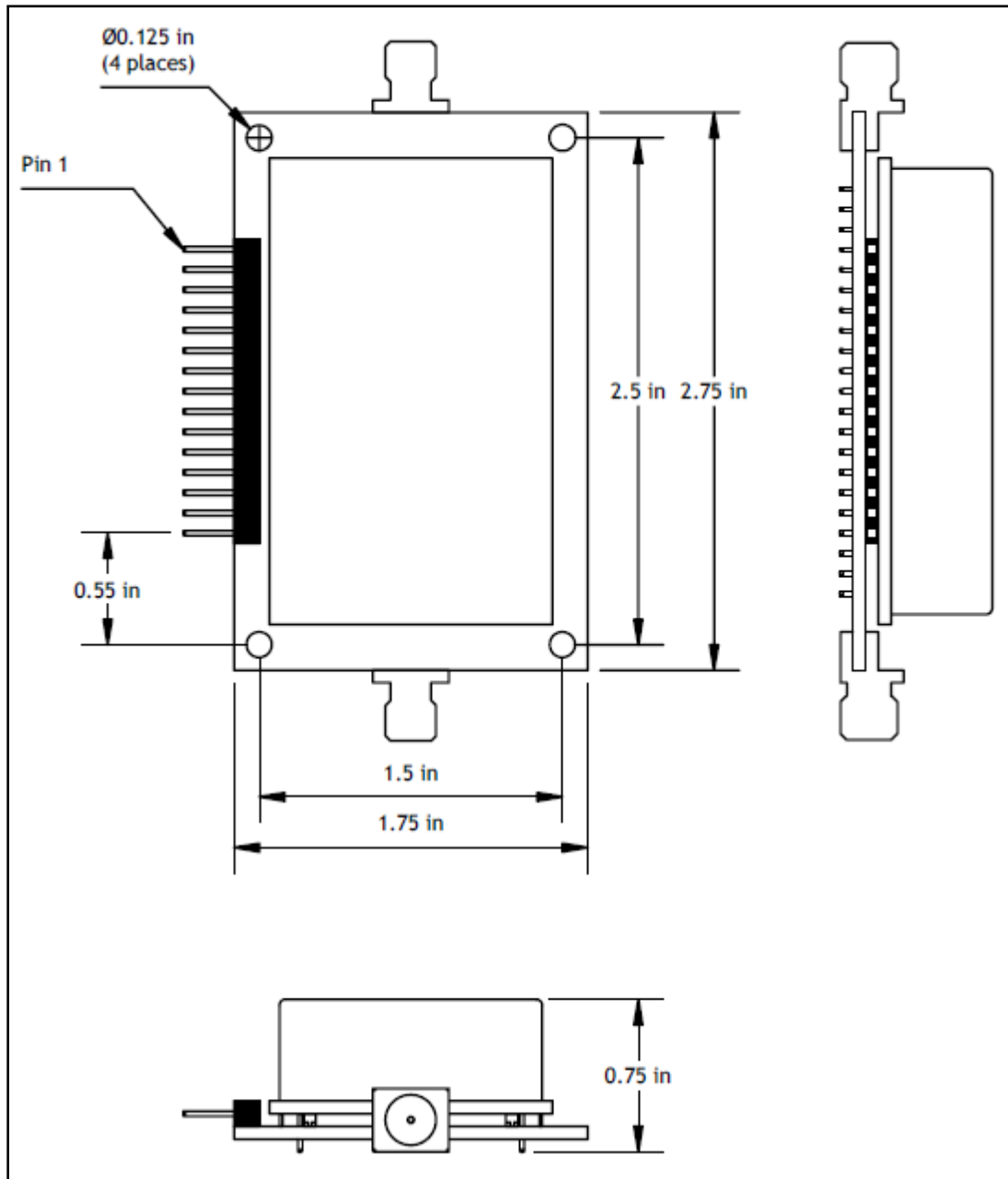


Figure 6: Connectorized SMA Package Dimensions, Top and Side Views

## APPLICATION INFORMATION

The power handling capability of the filter is dependent on VSWR, bandwidth, and bias voltage. Lower levels of bias voltage, all the way down to +10V are possible, as long as RF signal levels remain appropriately low. Power levels should be reduced to below 0dBm during switching.

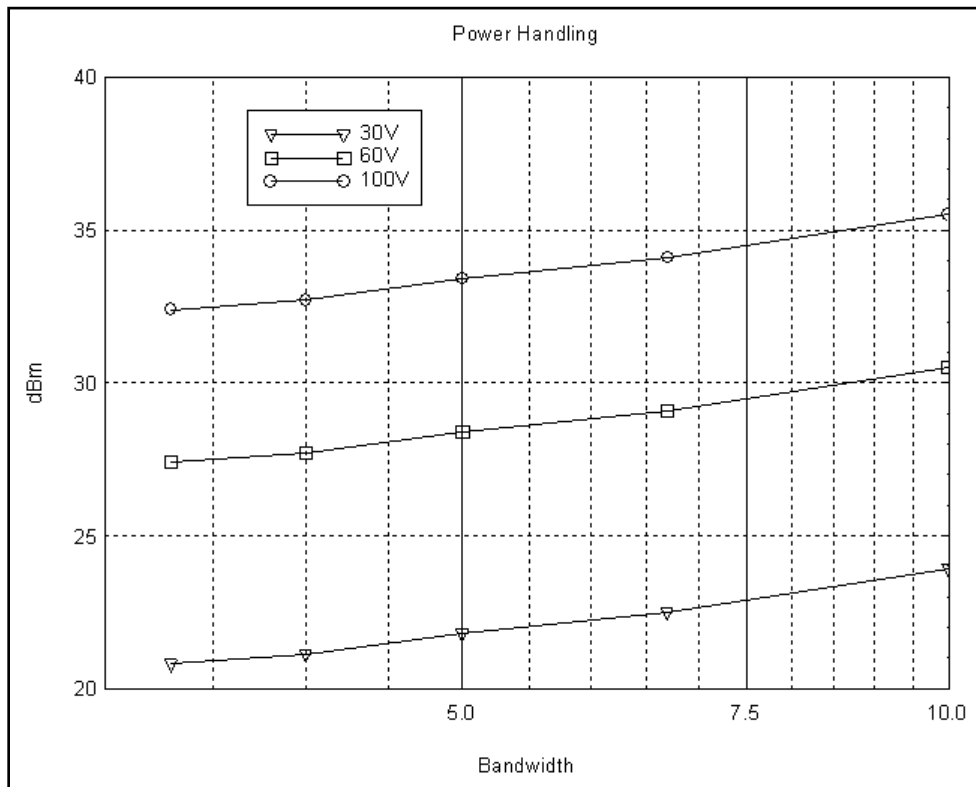


Figure 7: Power Handling versus Bias and Bandwidth

### SOLDERING

The TS-5010 should be hand soldered. Wave solder or IR reflow may cause parts on the internal circuit boards to loosen or shift position. The use of sockets is acceptable.

### NC PINS

Do not connect anything to the NC (no connect) pins. They are used for internal signaling (PIN diode drive voltages).

### PCB EDGES

The edges of the bottom circuit board have exposed inner layer traces (GND, V<sub>CC</sub>). Care must be taken such that they do not short to adjacent components.